23. The method of manufacturing a semiconductor device of claim 11, wherein the step of mounting a solder ball on said solder is performed after the step of cutting.--

REMARKS

Claims 1-6 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Inoue et al.. Claim 1 is independent. This rejection is respectfully traversed for the following reasons.

Claim 1 recites in pertinent part, "(b) forming a through-hole on the resin layer; (c) first cutting where one of the wafer and the resin layer is cut." Accordingly, claim 1 defines two ***distinct*** steps (b) and (c) which can be performed in a single process step or two different steps. Nonetheless, claim 1 expressly differentiates between the through-hole forming step and the cutting step, whereby the respective processes create a hole/cut that can serve different functions. For example, the through-hole can be used for connecting a semiconductor element to an external solder ball, whereas the cut derived from the "first cutting" can be used as a thermal distortion barrier. One of the purposes of the present invention is to provide a distinct cutting step which cuts the wafer and/or resin layer <u>in addition</u> to any hole producing process used to conduct the "forming a through-hole" step, in order to reduce thermal distortion (which can result from the different thermal expansion coefficients between the semiconductor wafer and resin layer) so that conductive balls can be easily and properly mounted on the resin.

The Examiner alleges that "Inoue et al. discloses forming through hole 3a in resin layer 3 ***by*** first cutting ... " (emphasis added). That is, the Examiner has interpreted the processing of aperture portions 3a as ***both*** the step of forming a through-hole and the step

of cutting. In other words, the Examiner has improperly interpreted step (c) of claim 1 as the means by which step (b) is performed, rather than interpreting step (c) as a cutting step in addition to and independent of whatever processing is used to form the through-hole.

However, although the "cutting" and "forming a through hole" can be performed during the same processing step, the two processes themselves are expressly claimed as distinct. Accordingly, Inoue et al. does not disclose a "first cutting" step in addition to the process (which can be another cutting step) used to form the through-holes 3a.

As anticipation under 35 U.S.C. § 102 requires that each and every element of the claim be disclosed in a single prior art reference, Akzo N.V. v. U.S. Int'l Trade Commission, 808 F.2d 1471 (Fed. Cir. 1986), and because Inoue et al. does not disclose or suggest each and every limitation recited in claim 1, it is submitted that Inoue et al. does not anticipate claim 1, nor any claim dependent thereon.

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, ***Hartness International Inc. v. Simplimatic Engineering Co.,*** 819F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as claim 1 is patentable for the reasons set forth above, it is respectfully submitted that dependent claims 2-8 which depend on claim 1 are also patentable. In addition, it is submitted that claims 2-8 are patentable based on their own merits by adding novel and non-obvious features to the combination.

Based on all the foregoing, it is submitted that claims 1-6 are patentable over Inoue et al.. Accordingly, it is respectfully requested that the rejection of claims 1-6 under 35 U.S.C. § 102, be withdrawn.

NEW CLAIMS

New claims 7-21 are submitted to be allowable over the cited prior art. Claim 7 recites in pertinent part, "cutting one of said resin layer and said semiconductor wafer along a dividing line into one of a plurality of resin layers on said semiconductor wafer and a plurality of semiconductor wafers on said resin layer, respectively." In contrast, each of the holes 3a are completely surrounded by resin layer 3 so that resin layer 3 is NOT cut into a ***plurality*** of pieces ***on the alleged semiconductor wafer***. That is, layer 3 of Inoue et al. is maintained as a single layer with holes formed therein until the device as a whole (including the alleged semiconductor wafer) is cut into a plurality of pieces.

The present invention as recited in claim 7 provides the capability of reducing heat-related distortion to the resin layer which can result from the differing thermal coefficient of expansion between the resin layer and semiconductor substrate. By dividing one of the two layers into a plurality of pieces, while placed on the other layer, the present invention can reduce such heat-related distortions so as to ease the process of mounting a solder ball on the conductive via.

Each of claims 8-21 add novel and non-obvious features to the combination.

CONCLUSION

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication for which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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